



## 8255 DATA SHEET

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purposes I/O component to Interface peripheral equipment to a microcomputer system bus. The functional configuration of the 8255A is programmed by software so that normally no external logic is necessary to interface peripheral devices or status

### Data Bus Buffer

This 3-state bi-directional 8-bit buffer is used to interface the 8255A to the systems data bus. Data transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

### Read/Write and Control Logic

The function of this block is to manage all of the Internal and External transfers of both Data and Status words. It accepts inputs from the CPU Address and Control bus and in turn, issues signals to both of the Control Groups.

#### (CS)

Chip Select. A  $\bar{CS}$  on this input pin enables the communication between the 8255A, and the CPU.

#### (RD)

Read. A  $\bar{RD}$  on this Input pin enables the 8255A to send the data or status information to the data bus. In essence, it allows the CPU to read from the 8255A.

#### (WR)

Write. A  $\bar{WR}$  on the input pin enables the CPU to write data or control words into the 8255A.

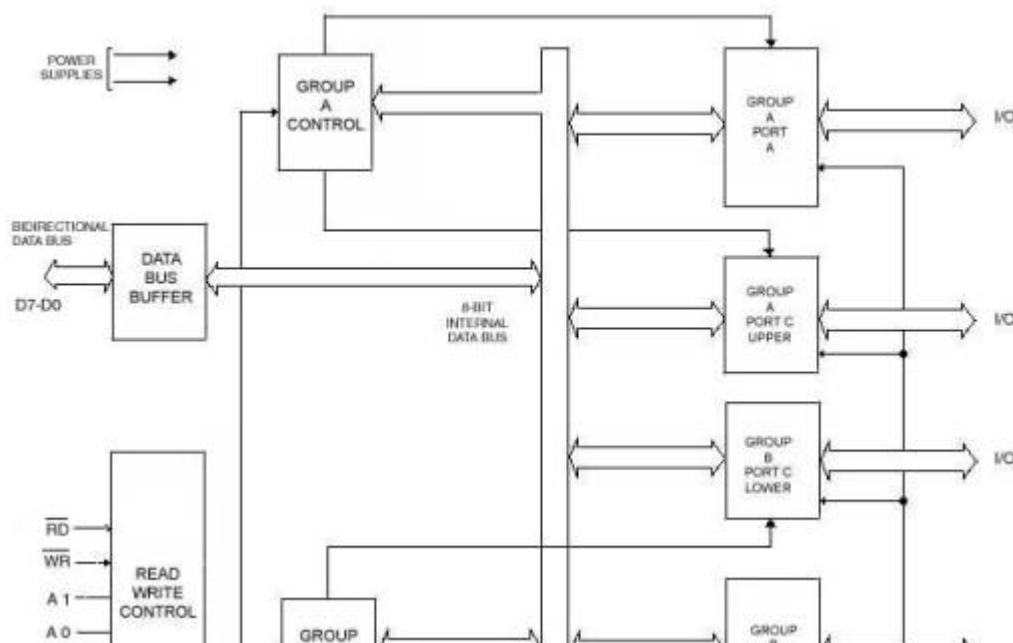
#### (A0 and A1)

Port Select 0 and Port Select 1. The Input signals, in conjunction with the RD and WR Input signals, select one of the three ports or the control word registers. They are normally connected to the significant bits of the address bus (A0 and A1).

### 8255A BASIC OPERATION

A1	A0	$\bar{RD}$	$\bar{WR}$	$\bar{CS}$	INPUT OPERATION (READ)
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0	0	0	1	0	PORT A $iV$ DATA BUS
0	1	0	1	0	PORT B $iV$ DATA BUS
1	0	0	1	0	PORT C $iV$ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS $iV$ PORT A
0	1	1	0	0	PORT B $iV$ DATA BUS
1	0	1	0	0	PORT C $iV$ DATA BUS
1	1	1	0	0	DATA BUS $iV$ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS $iV$ 3 STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS $iV$ 3 STATE



**Figure 3. 8255 A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic (RESET)**

**Reset.** A  $\bar{RST}$  on this Input clears the control register and all ports (A, B, C) are set to the Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence

output a control word to the 8255A. The control word contains information such as  $\overline{sm}$  reset, etc. that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts commands from the Read/Write receives control words from the internal data bus and issues the proper commands to its as

Control Group A  $\overline{V}$  Port A and Port C upper (C7 C4)

Control Group B  $\overline{V}$  Port B and Port C lower (C3 C0)

The Control Word Register can only be written into. No.

Read operation of the Control Word Register is allowed.

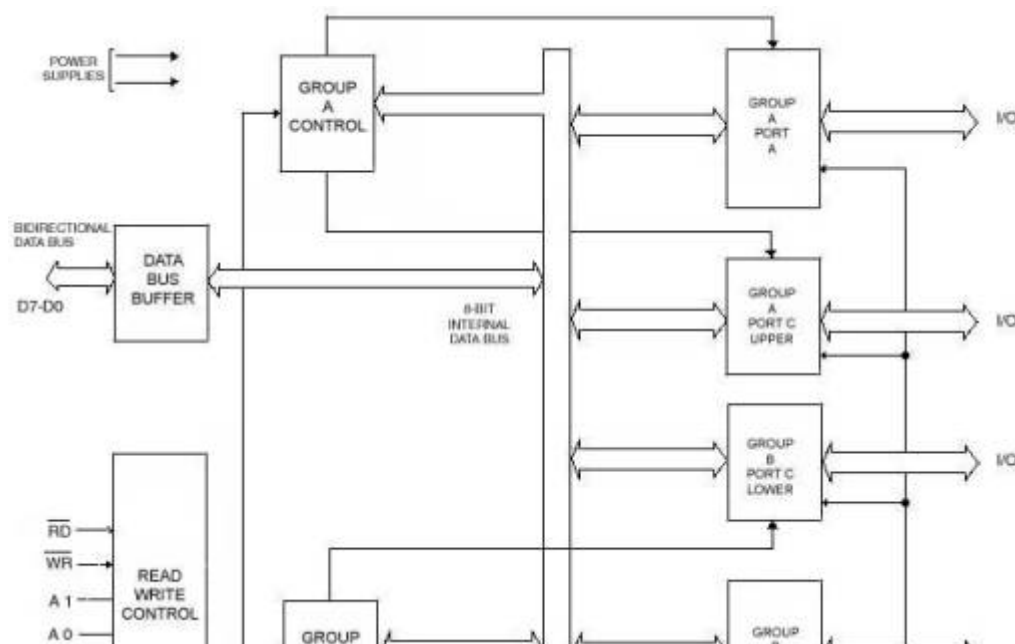
## Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of characteristics by the system software but each has its own special features or personally to the power and flexibility of the 8255A.

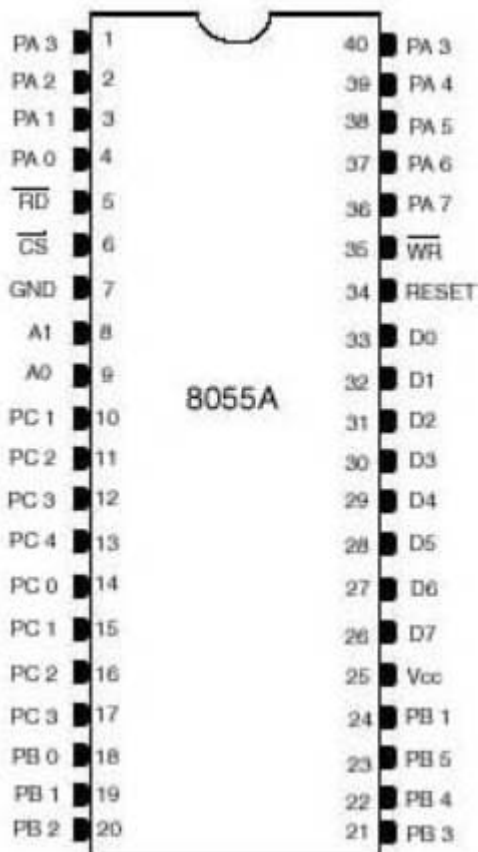
**Port A.** One 8-bit data output latch/buffer and one 8-bit data input latch.

**Port B.** One 8-bit data output latch/buffer and one 8-bit data input buffer.

**Port C.** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and for the controls signal outputs and status signal inputs in conjunction with ports A and B.



## PIN CONFIGURATION



D7 $\bar{}$ D0	DATA BUS DIRECTIONAL
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0 $\bar{}$ A1	PORT ADDRESS
PA 7 PA 0	PORT A (BIT)
PB 7 PB 0	PORT B (BIT)
PC 7 PC 0	PORT C (BIT)
Vcc	5 VOLTS
GND	0 VOLTS

## 8255A OPERATIONAL DESCRIPTION

### Mode Selection

There are three basic modes of operation that can be selected by the systems software:

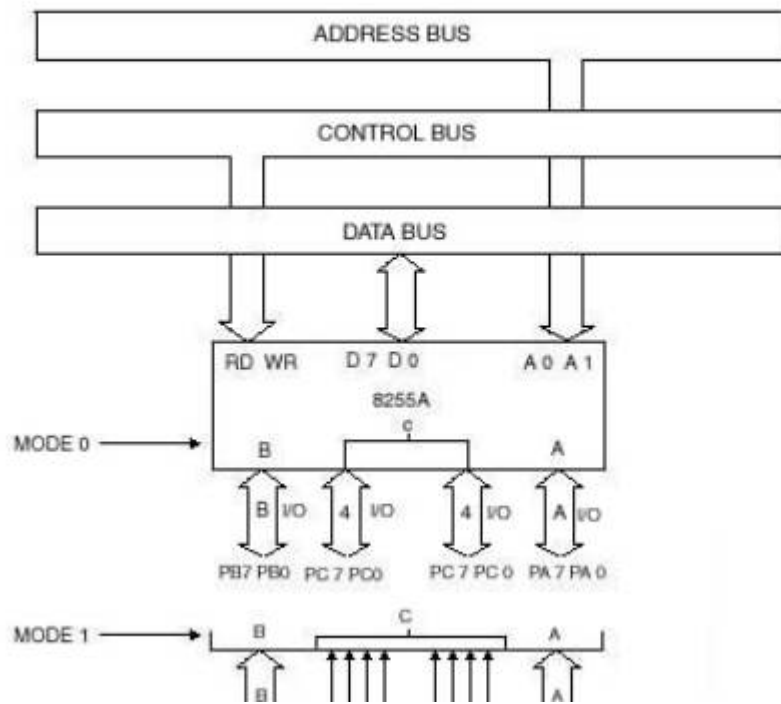
Mode 0  $\bar{}$  Basic Input/Output

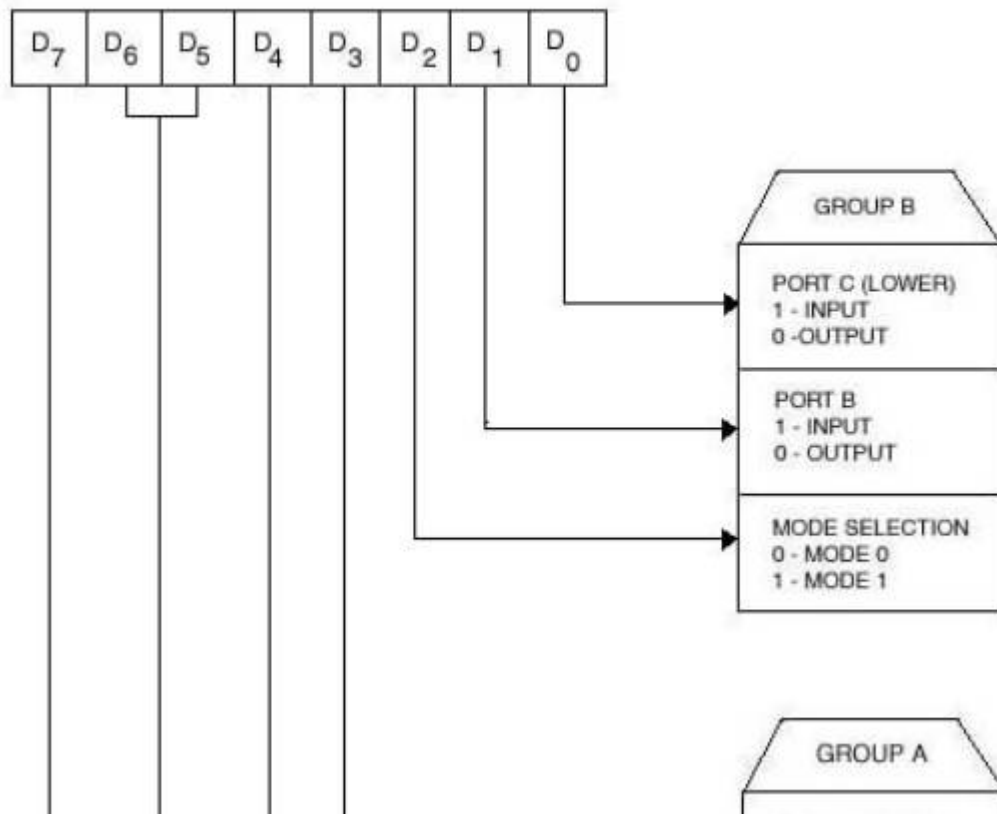
Mode 1  $\bar{}$  Strobed Input/Output

Mode 2  $\bar{}$  Bi-Directional Bus

When the reset Input goes  $\bar{}$ high $\bar{}$  all ports will be set to the Input mode (i.e., all 24 lines will be in an impedance state). After the reset is removed the 8255A can remain in the input mode with no further action required. During the execution of the systems program any of the other modes may be selected by the software. This allows a single 8255A to service a variety of peripheral devices with a minimum of maintenance routine.

The modes for Ports A and Port B can be separately defined, while Port C is divided into two groups, Group A and Group B. All of the output registers, including the status flip-flops, will be in the input mode if the mode is changed. Modes may be combined so that their functional definition can be  $\bar{}$ tailored $\bar{}$  to the system's requirements. For instance; Group B can be programmed in Mode 0 to monitor simple switch closure, Group A could be programmed in Mode 1 to monitor a keyboard or timer on an interrupt-driven basis.



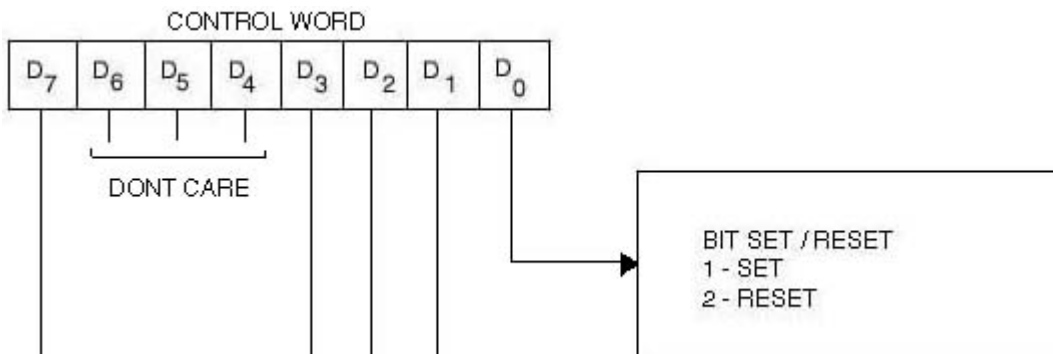


**Figure 6. Mode Definition Format**

The Mode definitions and possible mode combinations may seem confusing at first but after complete device operation a simple, logical I/O approach will surface. The design of the 8255 things such as efficient PC board layout, control signal definition vs PC layout and complete almost any peripheral device with no use of the available pins.

### Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUT put Instruction. This feature meets requirements in Control-based applications.



When Port C is being used as status/control for Port A or B these Bits can be set or reset by just as if they were data output port.

### Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided to the CPU. The interrupt request signal generated from port C, can be inhibited or enabled using the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the device in the interrupt structure.

#### INTE flip-flop definition

(BIT-SET)  $\bar{i}V$  INTE is SET  $iV$  Interrupt enable

(BIT-RESET)  $iV$  INTE is RESET  $\bar{i}V$  Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device reset.

#### Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input operations and output operations. No handshaking is required data is simply written to or read from a specified port.

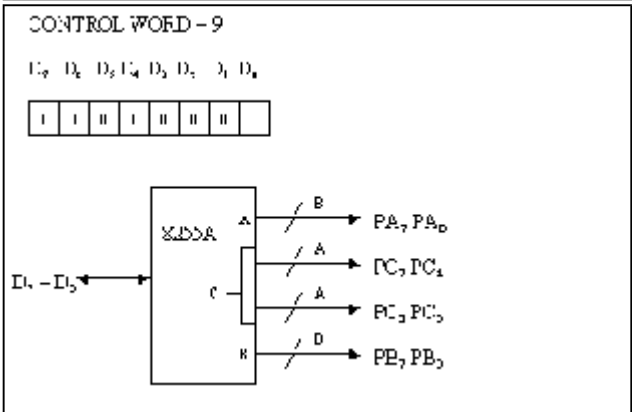
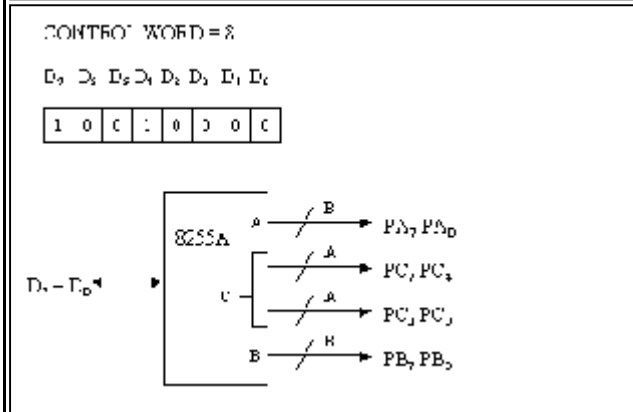
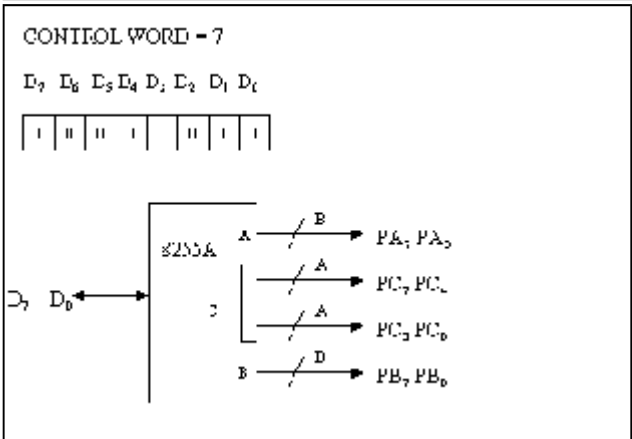
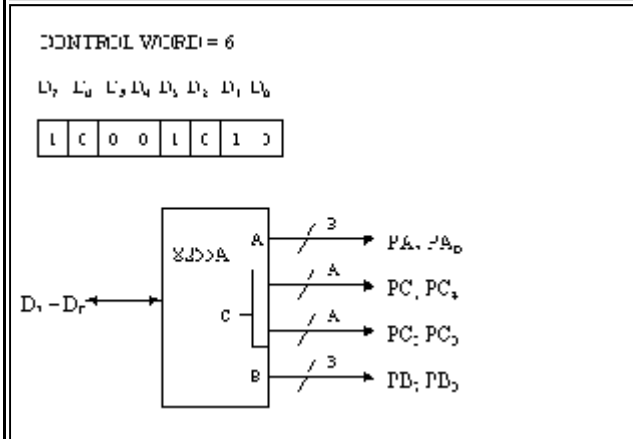
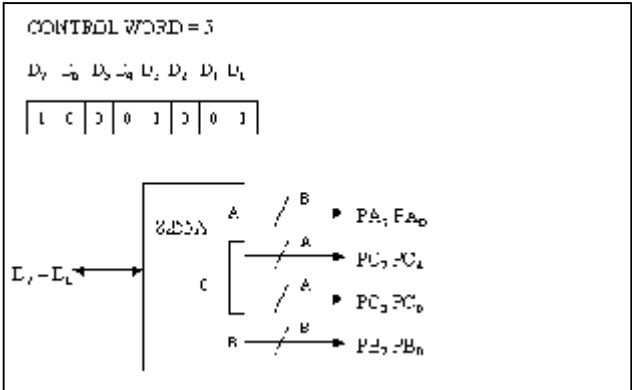
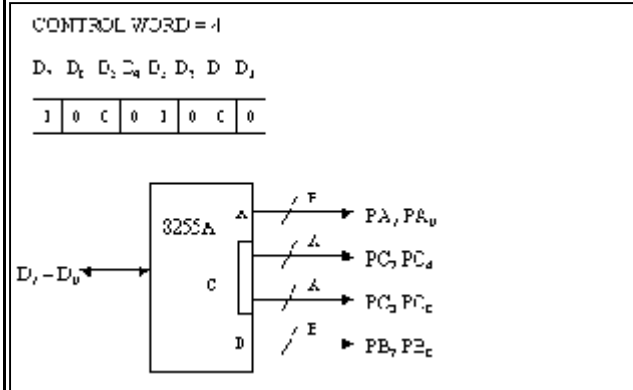
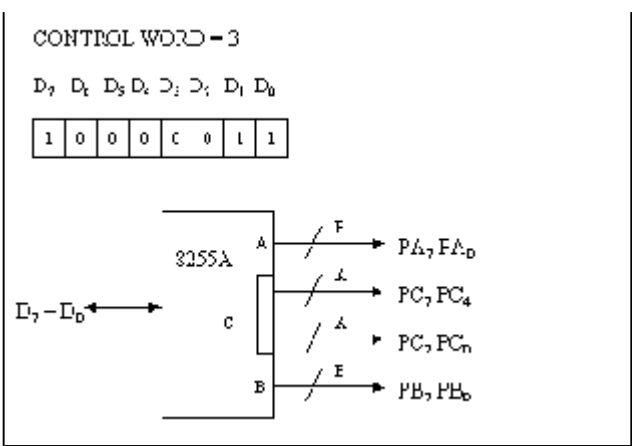
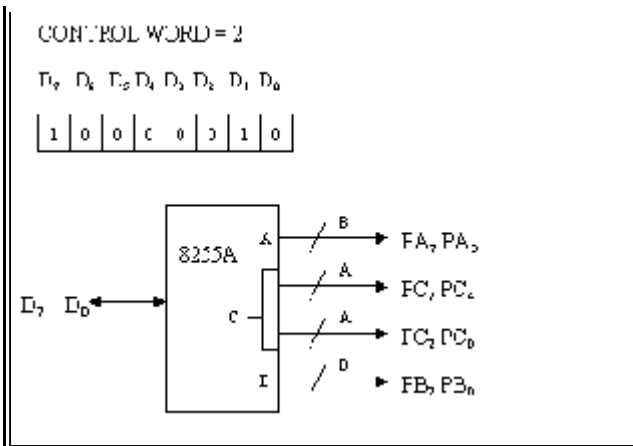
#### Mode 0 Basic Functional Definitions:

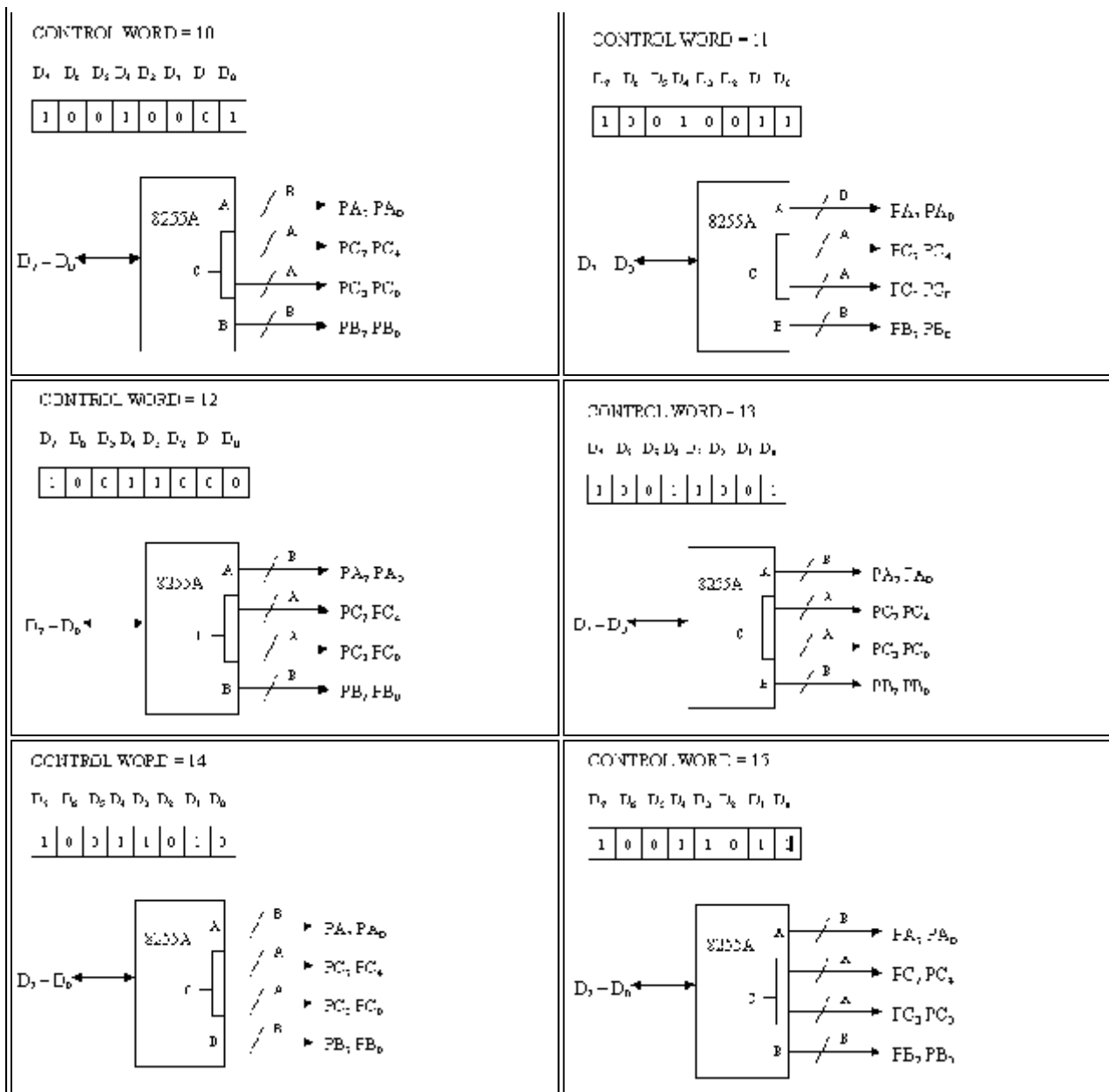
\*Two 8-bit ports and two 4-bit port

- \*Any port can be input or output.
- \*Outputs are not latched.
- \*Inputs are not latched.
- \*16 different Input/output configurations are not possible in this Mode.

A	B	GROUP A	GROUP B
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<b>Mode 0 Configuration</b>																				
<p>CONTROL WORD = 0</p> <p><math>E_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0</math></p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <tr> <td style="padding: 2px;">1</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">C</td> <td style="padding: 2px;">0</td> </tr> </table> 	1	0	0	0	0	0	0	0	C	0	<p>CONTROL WORD = 1</p> <p><math>D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0</math></p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <tr> <td style="padding: 2px;">1</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">0</td> <td style="padding: 2px;">1</td> </tr> </table> 	1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	C	0											
1	0	0	0	0	0	0	0	1												





## Operating Modes

**MODE 1 (Strobed Input/Output).** This functional configuration provides a means for transfer port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use or accept these "handshaking" signals.

### Mode 1 Basic Functional Definitions:

- \*Two groups (Group A and Group B)
- \*Each group contains one 8-bit data port and one 4-bit control/data port
- \*The 8-bit data port can be either Inputs or output Both inputs and outputs are latched.
- \*The 4-bit port is used for control and status of the 8-bit data port.

### Input Control Signal Definition

**STB (Strobe Input).** A "low" on the input loads data into the input latch.

**IBF (Input Buffer Full F/F)**

A "high" on this output indicates that the data has been loaded into the input latch. In essence IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

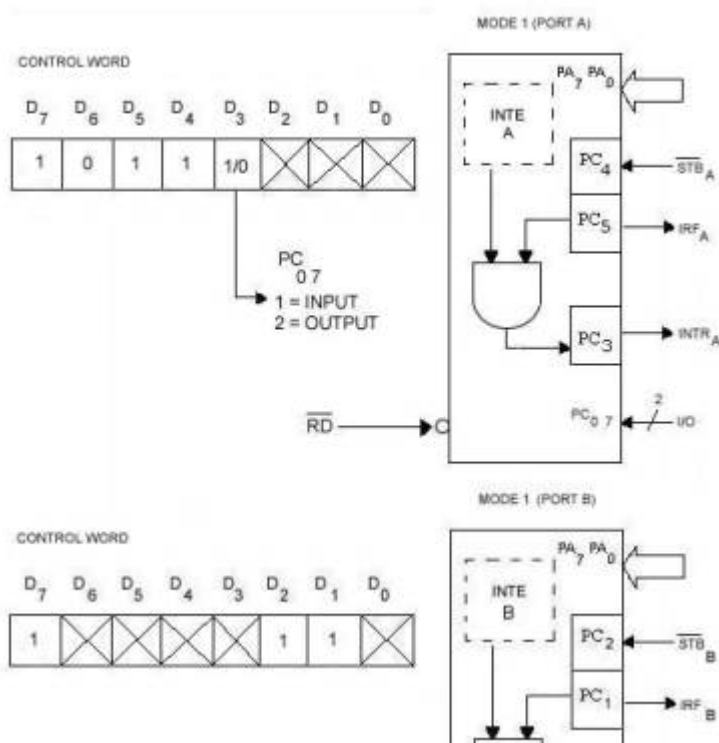
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. IBF is a "one" and INTE is "one". It is reset by the falling edge of RD. This device to request service from the CPU by simply strobing its data into port.

INTE A

Controlled by bit set/reset of PC4

INTE B

Controlled by set/reset PC2



## Output Control Signal Definition

**OBF (Output Buffer Full F/F).** The OBF output will go "low" to indicate that the CPU has The OBF F/F will be set by rising edge of the WR input being low.

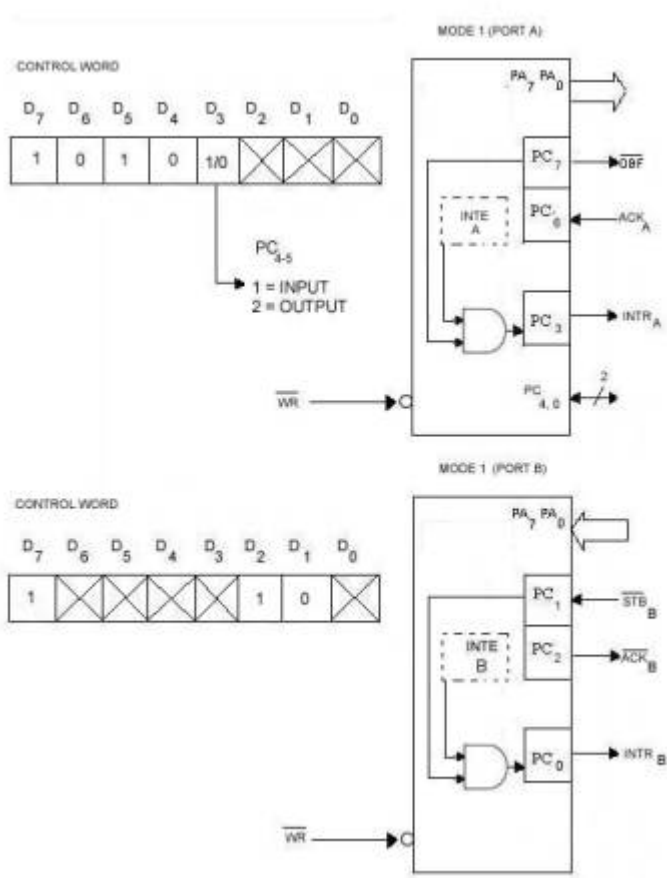
**ACK (Acknowledge Input).** A  $\bar{A}$  on this input informs the 8255A that the data from peripheral device, a response from the peripheral device indicating that it has received the data output.

**INTR (Interrupt Request).** A  $\bar{A}$  on the output can be used to interrupt the CPU when transmitted by the CPU. INTR is set when ACK is a  $\bar{A}$ , OBF is a  $\bar{A}$ , and INTE is a edge of WR.

INTE A

Controlled by bit set/reset of PC6.

INTE B

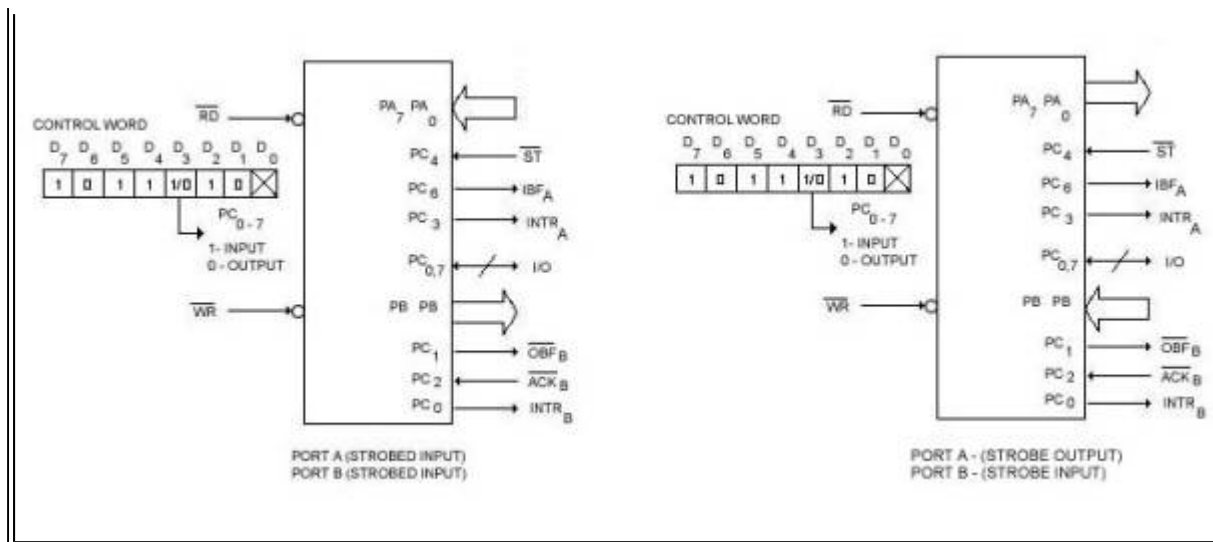


Controlled by bits of PC2.

**Combination of MODE 1**

Port A and B can be Individually defined as Input or output in Mode 1 to support a wide variety of peripheral devices.





**Mode 2 (Strobed Bidirectional Bus I/O).** This functional configuration provides a means for device or structure on a single 8-bit bus for both transmitting and receiving data (bi-direction) are provided to maintain proper bus flow discipline in a similar manner to MODE.

1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

\*Used in Group A only.

\*One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).

\*Both Inputs and Outputs are latched.

\*The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port.

### Bi-directional Bus I/O Control Signal Definition

**INTR (Interrupt Request).** A high on this output can be used to interrupt the CPU for both input and output operations.

### Output Operations

**OBF (Output Buffer Full).** The OBF output will go low to indicate that the CPU has written data to the output buffer.

**ACK (Acknowledge).** A high on this input enables the tri-state output buffer of port A to output data. When the output buffer is in the high impedance state, ACK is low.

**INTE 1 (The INTE Flip-Flop Associated with OBF).** Controlled by bit set/reset of PC6.

### Input Operations

#### STB (Strobe Interrupt)

**STB (Strobed Input).** A high on this input loads data into the input latch.

**IBF (Input Buffer Full F/F).** A high on this output indicates that data has been loaded into the input buffer.

**INTE 2 (The INTE Flip-Flop Associated with IBF).** Controlled by bit set/reset of PC4.

### Mode Definition Summary

**MODE 0**

**MODE 1**

**MODE 2**

### **Special Mode Combination Considerations**

There are several combinations or modes when not all of the bits in Port C are used for counting. The following modes can be used as follows:

If Programmed as Inputs-

All input lines can be accessed during a normal Port C read.

If programmed as Outputs-

Bits in C upper (PC7-PC4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC3\_Pco) can be accessed using the bit set/reset function or accessed as a

### Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and Ports C can source 1mA. The 8255A can directly drive Darlington type drivers and high-voltage displays that require such

### Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed for Mode 1, Port C generates or accepts handshake signals with the peripheral device. Reading the status information from Port C allows the programmer to test or verify the status of each peripheral device and change the program

There is no special instruction to read the status information from Port C. A normal read operation performs this function.

**Figure 17. MODE 1 STATUS WORD FORMAT**

#### INPUT CONFIGURATION

D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>

#### OUTPUT CONFIGURATION

D<sub>7</sub> D<sub>6</sub> D<sub>5</sub> D<sub>4</sub> D<sub>3</sub> D<sub>2</sub> D<sub>1</sub> D<sub>0</sub>

**Figure 18. Mode 2 Status Word Format**

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
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DEFINE BY MODE 0 MODE 1 SELECTION

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